IN THE CLAIMS

Please amend the claims as follows:

1. (original) A system for rendering an image for display, including:

- a texture memory (134) for storing texture maps in a mipmap structure; texels in a texture map being specified by a pair of u and v coordinates;

- a rasterizer (120) operative to, for a texel (u, v),

  - determine corresponding initial 4D mipmap levels (mml_u, mml_v);

  - determine a magnification factor representing a magnification that occurs when the texel is mapped to a corresponding pixel position on the display; and

  - determine corresponding final 4D mipmap levels in dependence on the determined initial 4D mipmap levels mml_u, mml_v, and the magnification factor; and

- a texture space resampler (132) for obtaining texture data from a texture map identified by the pair of final 4D mipmap levels;

- a texture mapper (140) for mapping the obtained texture data to corresponding pixel data defining the display image.

2. (original) A system as claimed in claim 1, wherein the magnification factor represents a magnification in a vertical direction indicated by coordinate v.

3. (original) A system as claimed in claim 2, wherein the rasterizer is operative to determine a final vertical 4D mipmap level $fmml_v$ by adjusting mml_v to identify a lower resolution vertical 4D mipmap level if the magnification factor is less than a predetermined threshold and maintaining the determined mml_v mipmap level otherwise.

4. (original) A system as claimed in claim 1, wherein:

- the texture memory is arranged to store the texture maps in a 4D mipmap structure; each texture map being identified by a pair of 4D mipmap levels;
- the texture space resampler is operative to on-the-fly reconstruct at least part of a texture map of a 4D mipmap identified by the pair of initial 4D mipmap levels from a texture map of a 4D mipmap in the texture memory identified by the pair of final 4D mipmap levels for use by the rasterizer.

5. (original) A system as claimed in claim 1, wherein:

- the texture memory is arranged to store the texture maps in a

3D mipmap structure; each texture map being identified by a respective 3D mipmap level *mml*;

- the texture space resampler is operative to on-the-fly reconstruct at least part of a texture map of an identified 4D mipmap from an associated 3D mipmap with level *mml* in the texture memory.

6. (currently amended) A system as claimed in ~~claims 3 and 5~~claim 3, wherein the 3D mipmap level *mml* of the associated 3D mipmap is given by MAX(mml_u, $fmml_v$).

7. (currently amended) A system as claimed in ~~claims 4 and 5~~claim 4, wherein the 3D mipmap level *mml* of the associated 3D mipmap is given by MIN(mml_u, $fmml_v$).

8. (currently amended) A system as claimed in ~~claims 4 and 5~~claim 4, wherein the 3D mipmap level *mml* of the associated 3D mipmap is determined in dependence on a predetermined maximum anisotropy level *a*.

9. (original) A system as claimed in claim 8, wherein the 3D mipmap level *mml* of the associated 3D mipmap is given by MAX(MAX(mml_u, $fmml_v$)-*a*, MIN(mml_u, $fmml_v$)).

10. (original) A computer including a central processing unit, a memory, a display, and a system as claimed in claim 1.

11. (original) A method of rendering an image for display, including:

- storing texture maps in a mipmap structure; texels in a texture map being specified by a pair of u and v coordinates;
- in a rasterization operation determining, for a texel (u, v):
  - corresponding initial 4D mipmap levels (mml_u, mml_v);
  - a magnification factor representing a magnification that occurs when the texel is mapped to a corresponding pixel position on the display; and
  - corresponding final 4D mipmap levels in dependence on the determined initial 4D mipmap levels mml_u, mml_v, and the magnification factor;
- in a texture space resampling operation, obtaining texture data for a texture map identified by the final 4D mipmap levels; and
- mapping the obtained texture data to corresponding pixel data defining the display image.

12. (original) A computer program operative to cause a processor to perform the method of claim 11.